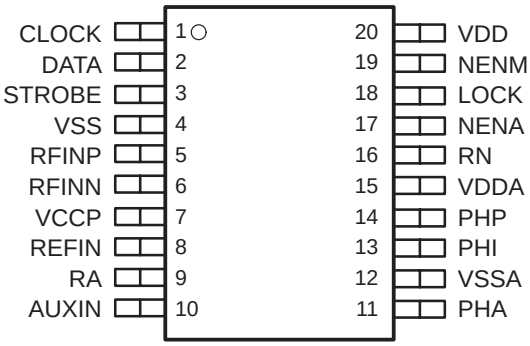
SLWS066 – JULY 1998

- **3-V Power Supply Operation**
- **2-GHz Operation**
- **Normal and Speed-Up Charge Pumps**
- **Dual PLL: One RF and One IF**
- **Additional, Directly Accessible Power-Down Modes**

PW PACKAGE
(TOP VIEW)



description

The TRF2052 is a dual-channel, low-power, phase-locked loop (PLL) frequency synthesizer component designed specifically for digitally enhanced cordless telephone (DECT) applications. The device is suitable for a variety of applications up through 2 GHz. A speed-up integral charge pump is used for fast channel switching. The simple serial interface is compatible with the extended performance mode (EPM) of other devices in Texas Instruments' synthesizer family.

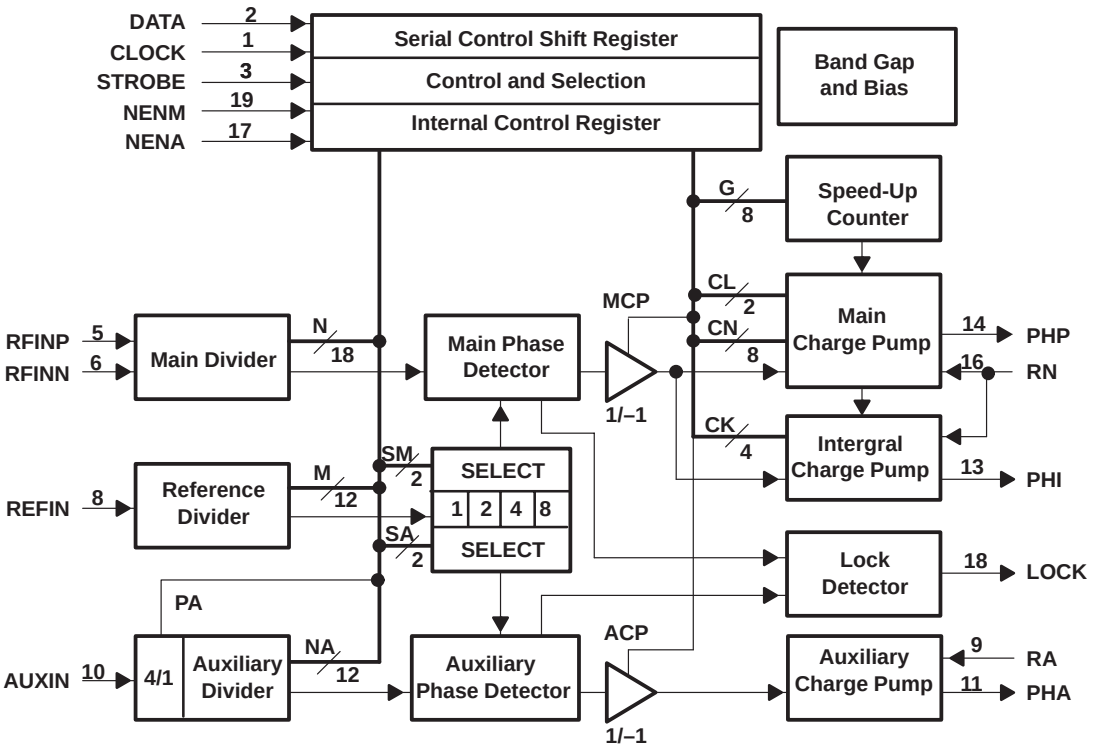
Along with the external loop filters, the TRF2052 provides all functions for voltage-controlled oscillators (VCO) in a dual-PLL frequency synthesizer system. A main channel is provided for RF frequencies and an auxiliary channel for IF frequencies. The current-output charge pumps directly drive passive RC filter networks, to generate VCO control voltages. Fast main-channel frequency switching is achieved with a charge pump arrangement that increases the current drive and alters the loop-filter frequency response during a portion of the switching interval.

The speed-up mode is controlled by the serial interface strobe signal, which goes high when a new frequency is loaded. At this time, the internal speed-up timer is activated and it enables the speed-up mode into the speed-up timer for the preprogrammed duration. During speed-up mode, the charge pump current to the external loop filter can be changed in two ways. First, the main charge pump current can be increased. Second, an additional integral charge pump can be separately and directly connected to the external loop-filter capacitor to further decrease the loop-filter charge and discharge times.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AUXIN	10	Auxiliary channel RF input
CLOCK	1	Serial interface clock signal
DATA	2	Serial interface data signal
LOCK	18	Lock detector output
NENA	17	Enable signal for the auxiliary channel/main channel/open loop. See modes of operation logic table. Active low
NENM	19	Enable signal for the auxiliary channel/main channel/open loop. See modes of operation logic table. Active low
PHA	11	Auxiliary charge pump output
PHI	13	Integral charge pump output
PHP	14	Main (proportional) charge pump output
RA	9	Resistor to VSSA sets auxiliary charge pump current
REFIN	8	Reference frequency input signal
RFINN	6	Prescaler negative RF input
RFINP	5	Prescaler positive RF input
RN	16	Resistor to VSSA sets main charge pump current
STROBE	3	Serial interface load signal
VCCP	7	Prescaler positive supply voltage
VDD	20	Digital supply voltage
VDDA	15	Analog supply voltage
VSS	4	Digital/prescaler ground
VSSA	12	Analog ground

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage range (See Note 1) . . . . . –0.6 to 4.7 Vdc
Input voltage, logic signals . . . . . –0.6 to 4.7 Vdc
Storage temperature range . . . . . –65°C to 150°C
ESD protection, all pins, human body model . . . . . 1 kV

NOTE 1: Voltage values are with respect to VSSA.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, VCCP, VDD, VDDA	2.7	3.3	V
Operating free-air temperature, T_A	–10	55	°C

dc electrical characteristics over full range of operating conditions, typical values are at VCCP = VDD = VDDA = 3 V, T_A = 25°C (unless otherwise noted)

supply current

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Average operational supply current (see Note 2)	EM = EA = 1 ES = 0 $\|I_{PHA}\|$ = 1 mA $\|I_{PHP\ N}\|$ = 0.5 mA $\|I_{PHP\ S}\|$ = 2.5 mA $\|I_{PHI}\|$ = 0 mA		11.4		mA

NOTE 2: Charge pump output current not included.

digital interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage (LOCK)	I_{OH} = 1 mA	V_{CC} – 0.5			V
V_{OL}	Low-level output voltage (LOCK)	I_{OL} = –1 mA			0.5	V
V_{IH}	High-level input voltage (DATA, CLOCK, STROBE, NENA, NENM)	I_{IH} = 10 μA	V_{CC} – 0.5			V
V_{IL}	Low-level input voltage (DATA, CLOCK, STROBE, NENA, NENM)	I_{IL} = 10 μA			0.5	V

ac electrical characteristics over full range of operating conditions, typical values are at VCCP = VDD = VDDA = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RF input frequency		0.1		2.0	GHz
Differential RF input voltage		–16		–3	dBm
Reference input frequency			13.8		MHz
Reference input voltage		0.3			V_{pp}
Auxiliary input frequency	(see Note 3)			150	MHz
Auxiliary input voltage		0.2			V_{pp}

NOTE 3: Used with predivider (1/4)

charge pump output currents

The steepness of the phase detector charge-pump chains is determined by external resistors between the dedicated pins RA and RN and ground, as well as by user programmable variables. The charts that follow indicate how the charge-pump peak currents can be set by the external resistors and the control variables.

auxiliary charge pump

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert I_{PHA} \rvert$	Open loop mode (NENA = 1)	$0 \le V_{PHA} \le V_{DDA}$		10		pA
$\lvert I_{PHA} \rvert$	Closed loop mode (NENA = 0)	$0.5\ V \le V_{PHA} \le V_{DDA} - 0.5\ V$, $R_A \ge = 18\ k\Omega$		$20 \times 1.25/R_A[k\Omega]$		mA

main charge pump

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert I_{PHM\_N} \rvert$	Normal mode	$0.5\ V \le V_{PHP} \le V_{DDA} - 0.5\ V$, $R_N \ge = 18\ k\Omega$		$18.75/(R_N[k\Omega] + 0.75) \times CN/256$		mA
$\lvert I_{PHM\_S} \rvert$	Speed-up mode (see Note 4)			$\lvert I_{PHM\_N} \rvert \times (1 + 2^{CL + 1})$		mA

4. The maximum allowable current is 12 mA. It is recommended to use the speedup mode only before the PLL is locked. Switching between speedup and normal modes as well as changing the current setting factor CN, under PLL operation, may cause disturbances in the VCO control voltage.

integral charge pump

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert I_{PHI\_N} \rvert$	Normal mode	$0 \le V_{PHI} \le V_{DDA}$		0		mA
$\lvert I_{PHI\_S} \rvert$	Speed-up mode (see Note 5)	$0.5\ V \le V_{PHI} \le V_{DDA} - 0.5\ V$, $R_N \ge = 18\ k\Omega$, $\lvert I_{PHM\_S} \rvert \le 16\ mA$		$\lvert I_{PHM\_N} \rvert \times 2^{CL + 1} \times CK$		mA

5. Maximum allowable current is 24 mA

The instantaneous values of the charge pump currents are related to the phase error by:

$$I_{PH\_inst} = \frac{\Theta_{error}}{2\pi} \times I_{PH\_peak} \qquad (1)$$

modes of operation†

CHIP MODE	NENM	NENA	ACTIVE STAGES
Both synthesizers on	0	0	Everything on
Main synthesizers on	0	1	Only auxiliary charge pump set to triple state; everything else working
Auxiliary synthesizer on	1	0	Main loop disabled, auxiliary loop working
Shutdown	1	1	All off

† Enable signals, NENM and NENA, are active low.

timing requirements, serial data interface (see Figure 1)

PARAMETER		MIN	MAX	UNIT
$f_{(CLOCK)}$	Clock frequency		10	MHz
$t_{w(CLKHI)}$	Clock high-time pulse width, Clock high	30		ns
$t_{w(CLKLO)}$	Clock low-time pulse width, Clock low	30		ns
$t_{su(D)}$	Set-up time, data valid before CLOCK↑	30		ns
$t_{h(D)}$	Hold time, data valid after CLOCK↑	30		ns
$t_{su(STROBE)}$	Set-up time, STROBE↑ before CLOCK↑	30		ns
$t_{w(STROBEHI)}$	STROBE high-time pulse width, STROBE high	30		ns
$t_{w(STROBELO)}$	STROBE low-time pulse width, STROBE low	30		ns

PARAMETER MEASUREMENT INFORMATION

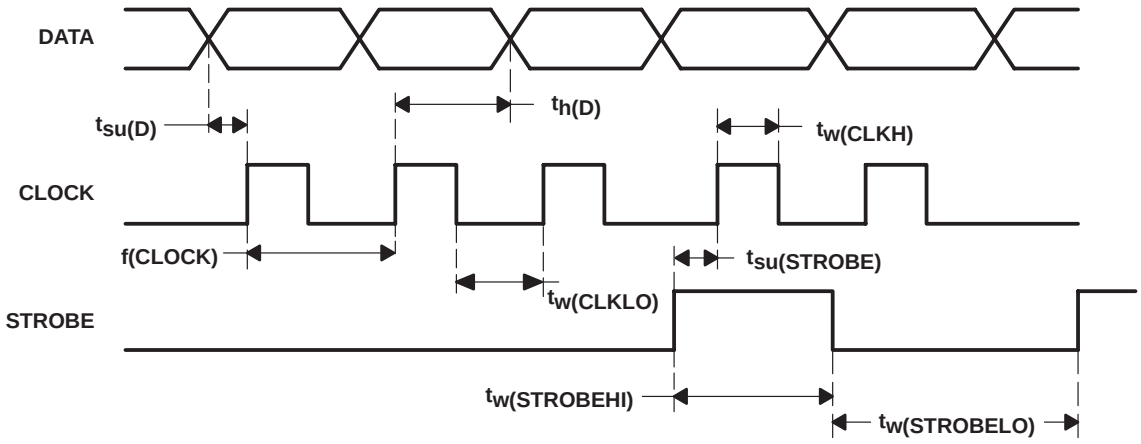


Figure 1. Serial-Data Interface Timing

PRINCIPLES OF OPERATION

serial control

The TRF2052 internal registers contain all the user programmable variables such as divider ratios, charge pump settings, etc. They are programmed using a three-wire (CLOCK, DATA, STROBE) serial interface.

At every rising slope of the CLOCK signal, the actual logical value on the DATA pin is written into a 24-bit shift register. A rising slope on the STROBE pin causes the actual content of the shift register to be input as a control word.

The control word is, therefore, 24-bits long and the first incoming bit functions as the least significant bit (LSB), bit 0. If the most significant bit (MSB), bit 23, is 1, the word functions as control word A. If the MSB is 0, bits 20 to 22 become address bits, which label the words as control word B through E, respectively. To fully program the synthesizer, four words must be sent: A, B, C, and D. Word E is for test purposes only.

The position of the individual variables within the control words is illustrated in Figure 2. Table 1 briefly describes their functions. The G parameter, which specifies the duration of the speed-up mode in reference divider cycles, splits into most significant (G2) and least significant (G1) nibbles.

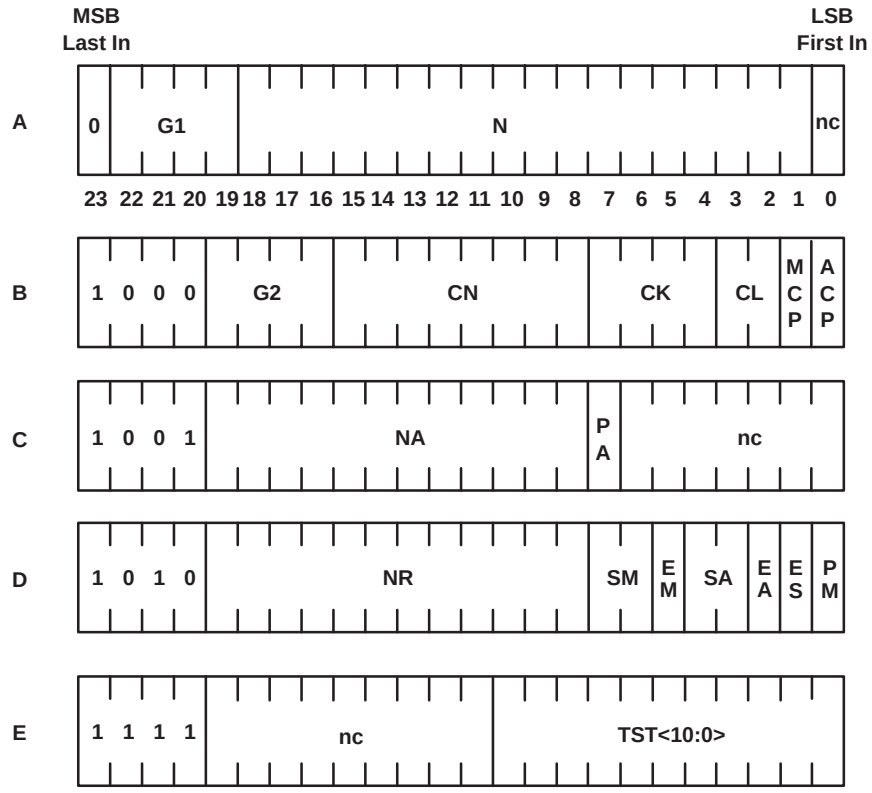


Figure 2. Serial Word Format

PRINCIPLES OF OPERATION

Table 1. Function Table

SYMBOL	BITS	FUNCTION
N	18	Overall main divider integer division ratio
CN	8	Binary current setting factor for main charge pumps
G2	4	MS bits for the speed-up mode duration (number of reference divider cycles)
G1	4	LS bits for the speed-up mode duration (number of reference divider cycles)
CK	4	Binary acceleration factor for integral charge pump current
CL	2	Binary acceleration factor for increase in main charge pump current during speed-up mode
MCP	1	Main charge pump polarity
ACP	1	Auxiliary charge pump polarity
NA	12	Auxiliary divider ratio
PA	1	Auxiliary prescaler select: 0 = divide by 4 1 = divide by 1
NR	12	Reference divider ratio
SM	2	Reference select for main phase detector
EM	1	Main divider enable flag
SA	2	Reference select for auxiliary phase detector
EA	1	Auxiliary divider enable flag
ES	1	Speed-up mode standby control: 0 = speed-up charge pump switches off completely if no fast mode 1 = speed-up charge pump always in standby
PM	1	Phase detector mode. Change between two modes for reset pulse generation: 0 = analog internal generated delay 1 = high-pulse duration for REF-CLOCK

RF inputs

The differential main divider input has a resistance of several kΩ and can be matched to the system impedance by an external resistor. To form a single ended input, any one of the input pins can be grounded by a blocking capacitor.

The auxiliary channel RF and reference inputs have a high resistance, as well, and are single ended. If needed, matching can be accomplished with an external resistor.

enabling the PLLs

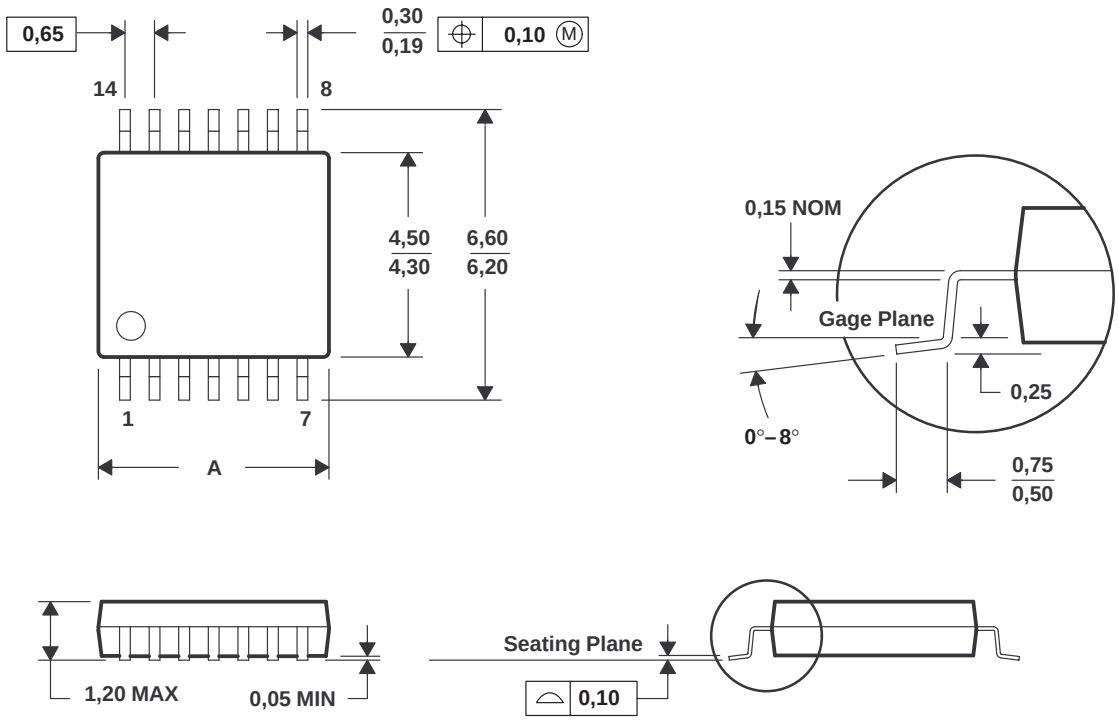
Both PLLs can be enabled and disabled independently, either by the serial control variables EM and EA or by the digital inputs pins NENM and NENA.

The serial control variables and the hardware signal NENM disable the charge pump and the divider of the corresponding loop, while NENA affects the auxiliary charge pump output only. This helps to avoid spikes that might occur after re–enabling the auxiliary loop by the serial interface.

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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